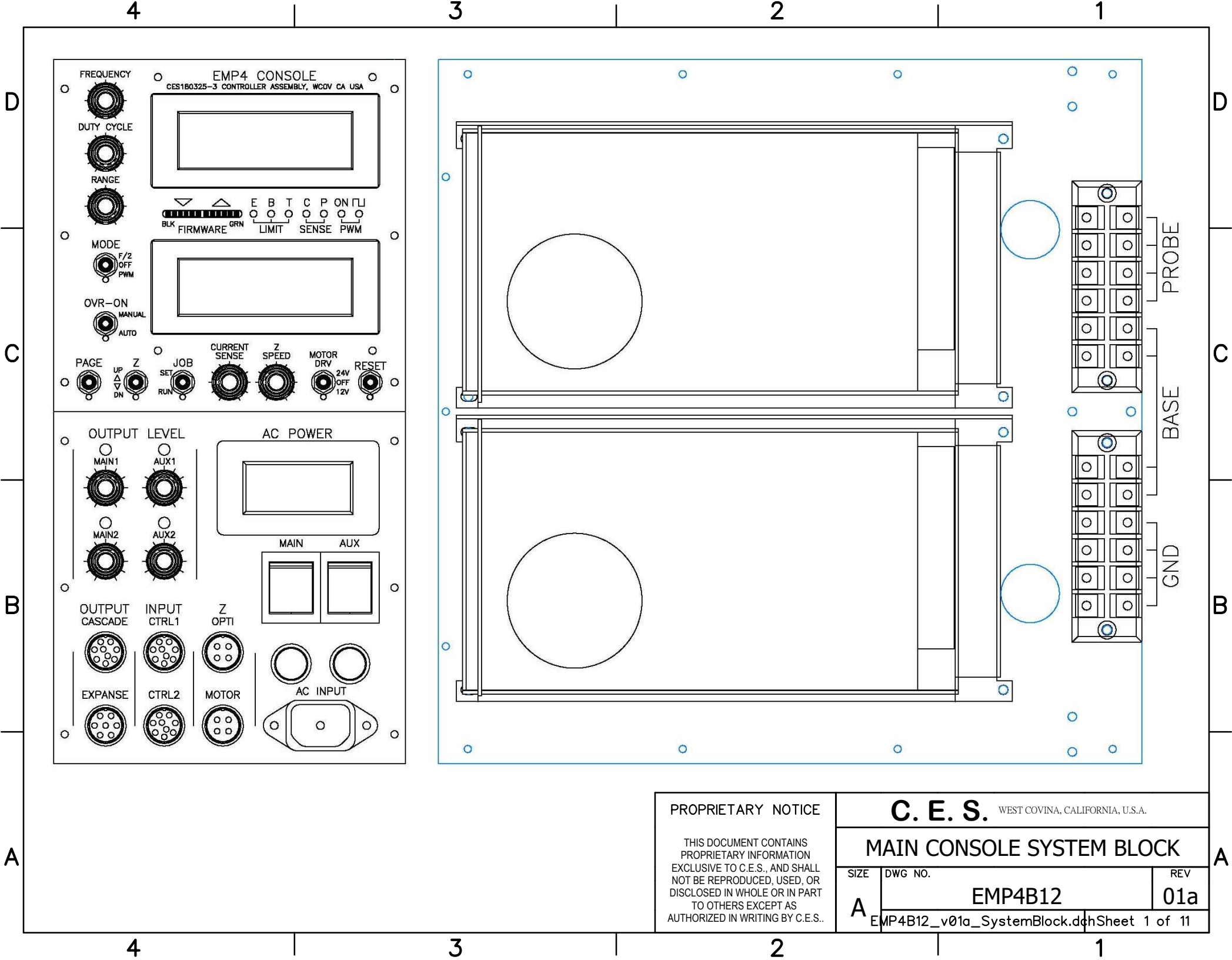
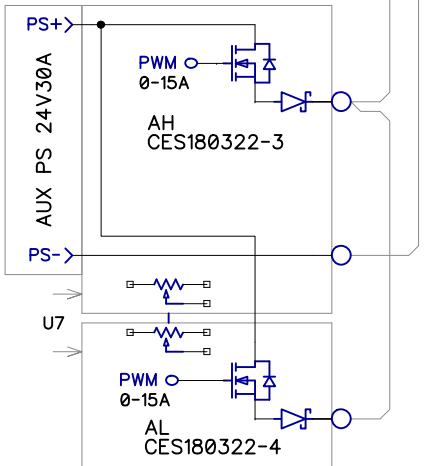
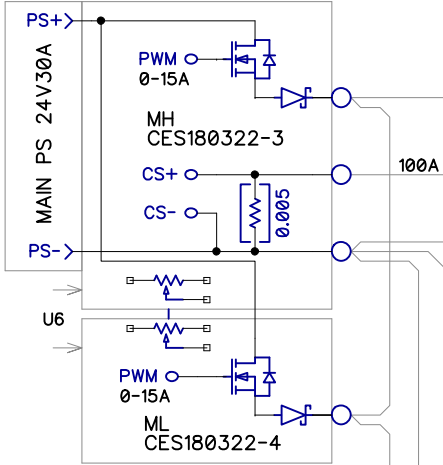




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		MAIN CONSOLE SYSTEM BLOCK	
		SIZE A	DWG NO. EMP4B12
		EMP4B12_v01a_SystemBlock.dchSheet 1 of 11	

EMP4



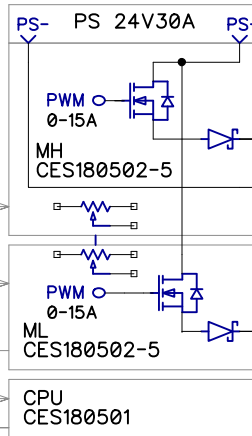
CASCADE-OUT
GX16-9
pin 1 +15V(FL)
pin 2 0V(FL)
pin 3 GATE(HI)
pin 4 +15VCC
pin 5 GATE(LO)
pin 6 SYS-GND
pin 7 RXD
pin 8 TXD
pin 9 EDM_ON-

EXPANSION-OUT
GX16-7
pin 1 +15VCC
pin 2 GATE(LO)
pin 3 SYS-GND(RX-)
pin 4 RXD/RX+
pin 5 TXD/TX-
pin 6 +5VCC(TX+)
pin 7 EDM_ON-

CASCADE
GX16
9

EXPANSION
GX16
7

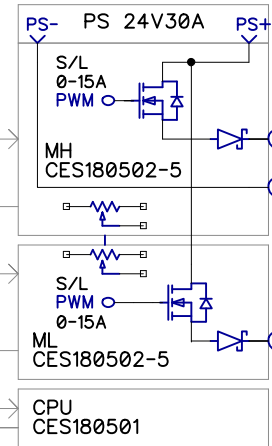
ECP4



CASCADE-IN
GX16-9
pin 1 +15V(FL)
pin 2 0V(FL)
pin 3 GATE(HI)
pin 4 +15VCC
pin 5 GATE(LO)
pin 6 SYS-GND
pin 7 RXD
pin 8 TXD
pin 9 EDM_ON-

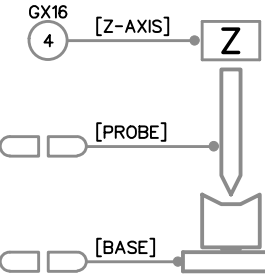
CASCADE-OUT
GX16-9
pin 1 +15V(FL)
pin 2 0V(FL)
pin 3 GATE(HI)
pin 4 +15VCC
pin 5 GATE(LO)
pin 6 SYS-GND
pin 7 RXD
pin 8 TXD
pin 9 EDM_ON-

EXP4



EXPANSION-IN
GX16-7
pin 1 +15VCC
pin 2 GATE(LO)
pin 3 SYS-GND(RX-)
pin 4 RXD/RX+
pin 5 TXD/TX-
pin 6 +5VCC(TX+)
pin 7 EDM_ON-

EXPANSION-OUT
GX16-7
pin 1 +15VCC
pin 2 GATE(LO)
pin 3 SYS-GND(RX-)
pin 4 RXD/RX+
pin 5 TXD/TX-
pin 6 +5VCC(TX+)
pin 7 EDM_ON-



EDMP4 SYSTEM CONFIG

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MAIN CONSOLE SYSTEM BLOCK

SIZE	DWG NO.	REV
A	EMP4B12	01a

EMP4B12_v01a_SystemBlock.dcr Sheet 2 of 11

4

3

2

1

D

D

C

C

B

B

A

A

SPS-SUB (S2) JP36
+24VIN +



+24V + JP37



SPS-SUB (S5) JP35
+15VIN +

ML-VCC JP42
+15VOUT +

AL-VCC JP43
+15VOUT +

+24V JP38

VOUT

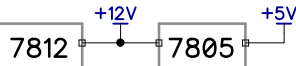
+12V JP40
+5V JP41

(opt)
PWM_Output JP8

SENSE

SENSE ADJ
5K POT

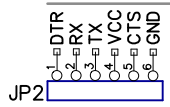
CPU Logic JP14
+15VIN +



EXPANSION HEADER

- D2_DS1820
- D3_PWM-OUT
- D4_MODE-SW
- D5_DRV-OFF
- D6_PWM-OFF
- D7_FREQ-OFF
- D8_TDX
- D9_RDX

CASCADE (F2) GX16-9
PIN.9
PIN.8



FIRMWARE PORT
P0325-Pxx_vnn

PWMGEN

(TO ZDRV D17)

- A3_PRESCALE-ADJ
- A2_DMA-CS
- A1_DMV-PB
- A0_DMV-PS
- D13
- D12_RUN
- D11_FREQ-OUT
- D10_EDM-ON

A3_PRESCALE-ADJ JP1
+5V I
5K POT

A7_FREQ-ADJ JP3
+5V I
5K POT

A6_DUTY-ADJ JP4
+5V I
5K POT

A4_SDA JP7
A5_SCL JP4
+5V I

D2_DS1820 JP5
+5V I

D2_DS1820 JP6
+5V I

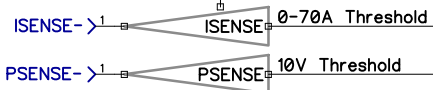
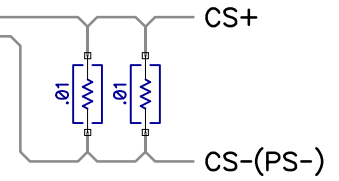
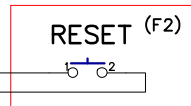
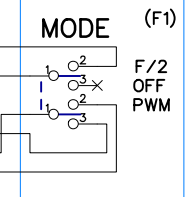
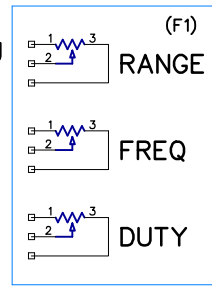
D4_MODE-SW JP12
F/2 CT

D3_PWM-OUT JP9
D6_PWM-OFF JP9
D11_FREQ-OUT JP9
D7_FREQ-OFF JP9

PWMGEN_CPU_RESET JP13
(SHT2) ZDRV_CPU_RESET

- A0_DMV-PS FS=200VDC
- A1_DMV-PB FS=200VDC
- A2_DMA-CS FS=95ADC

JP15
PS+
PROBE
CS+
CS-(PS-)



(F1) CES180325-3 PCB ASSEMBLY

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	MAIN CONSOLE SYSTEM BLOCK		
	SIZE	DWG NO.	REV
	A	EMP4B12	01a
	EMP4B12_v01a_SystemBlock.dwg Sheet 3 of 11		

D

D

C

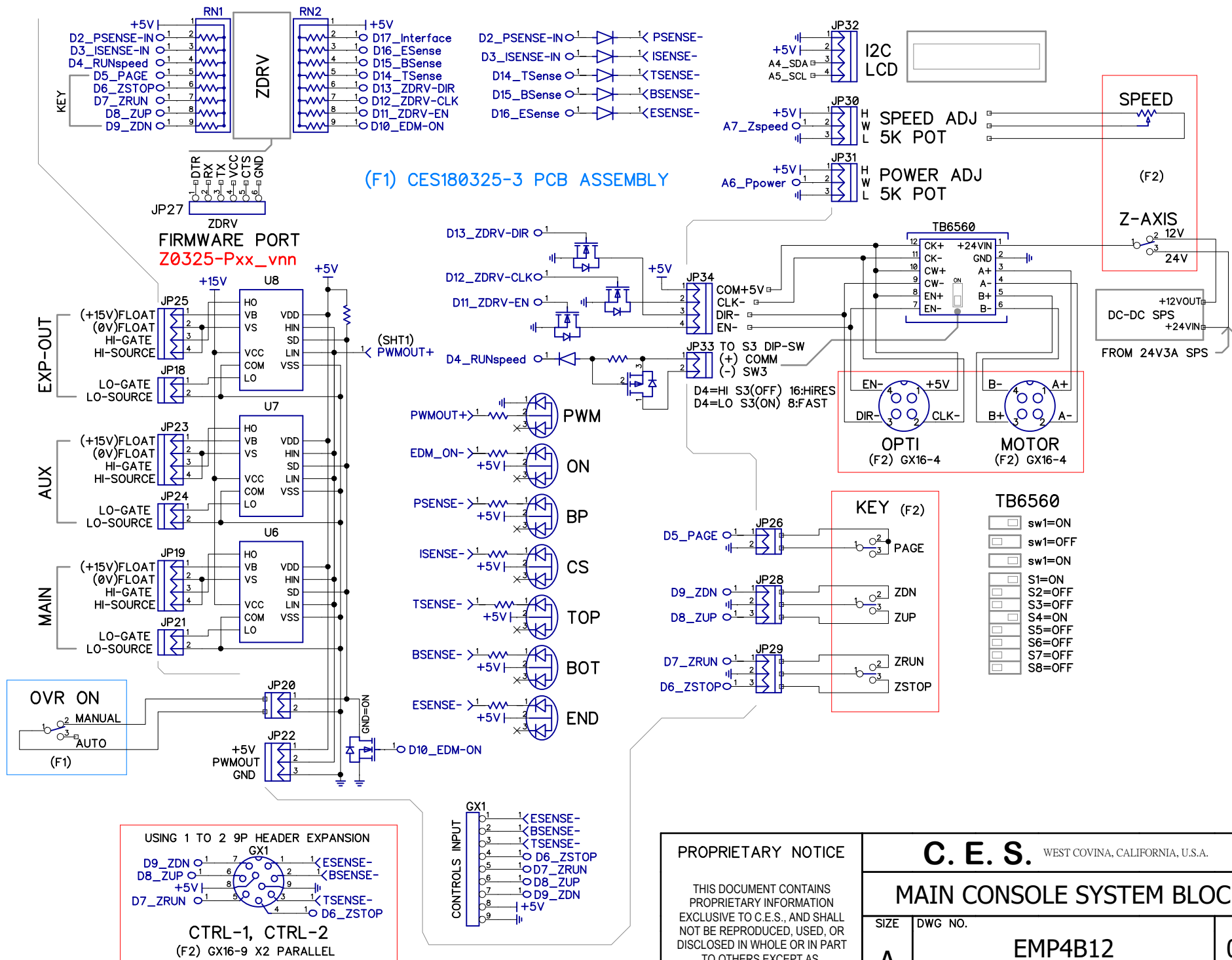
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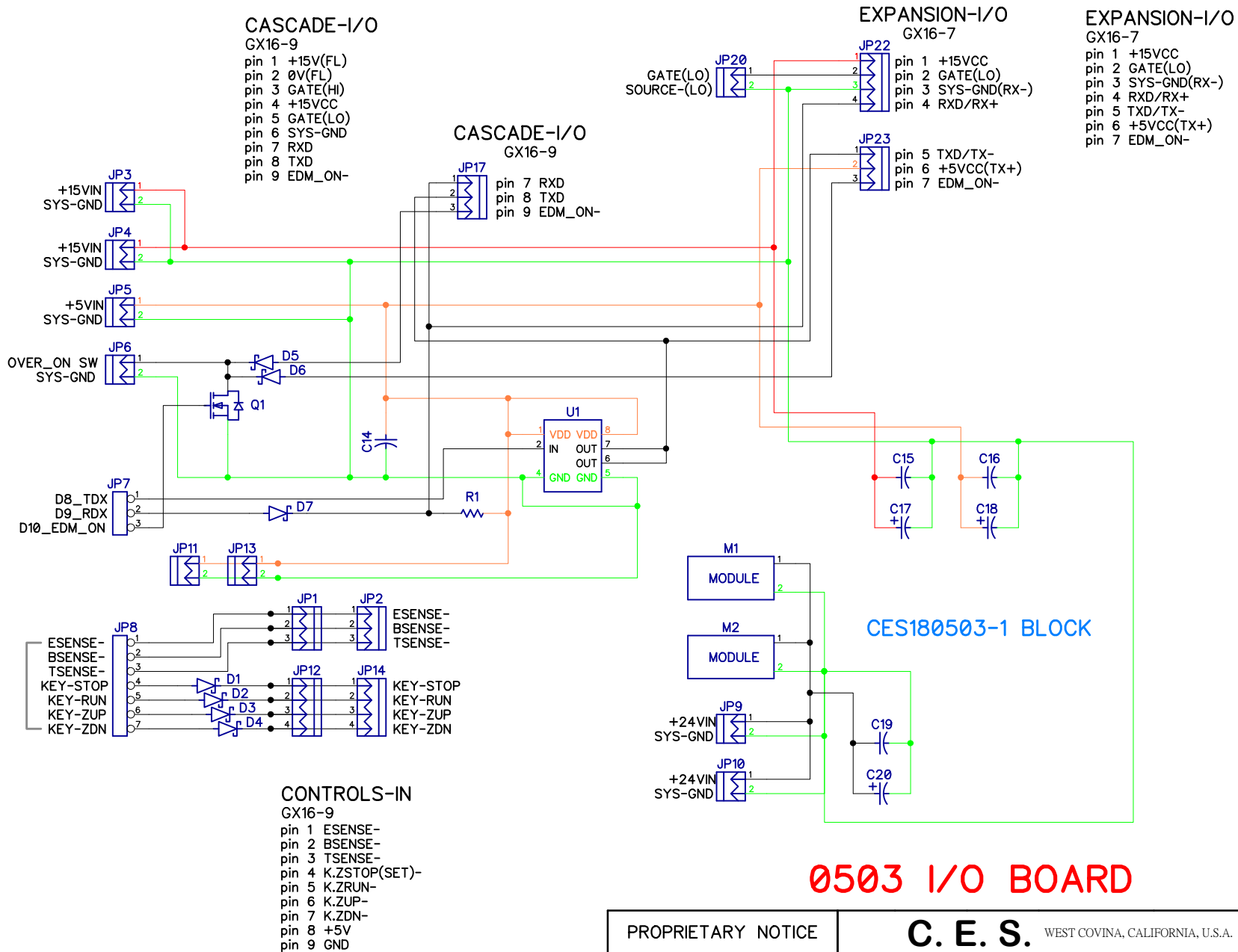
B

B

A

A





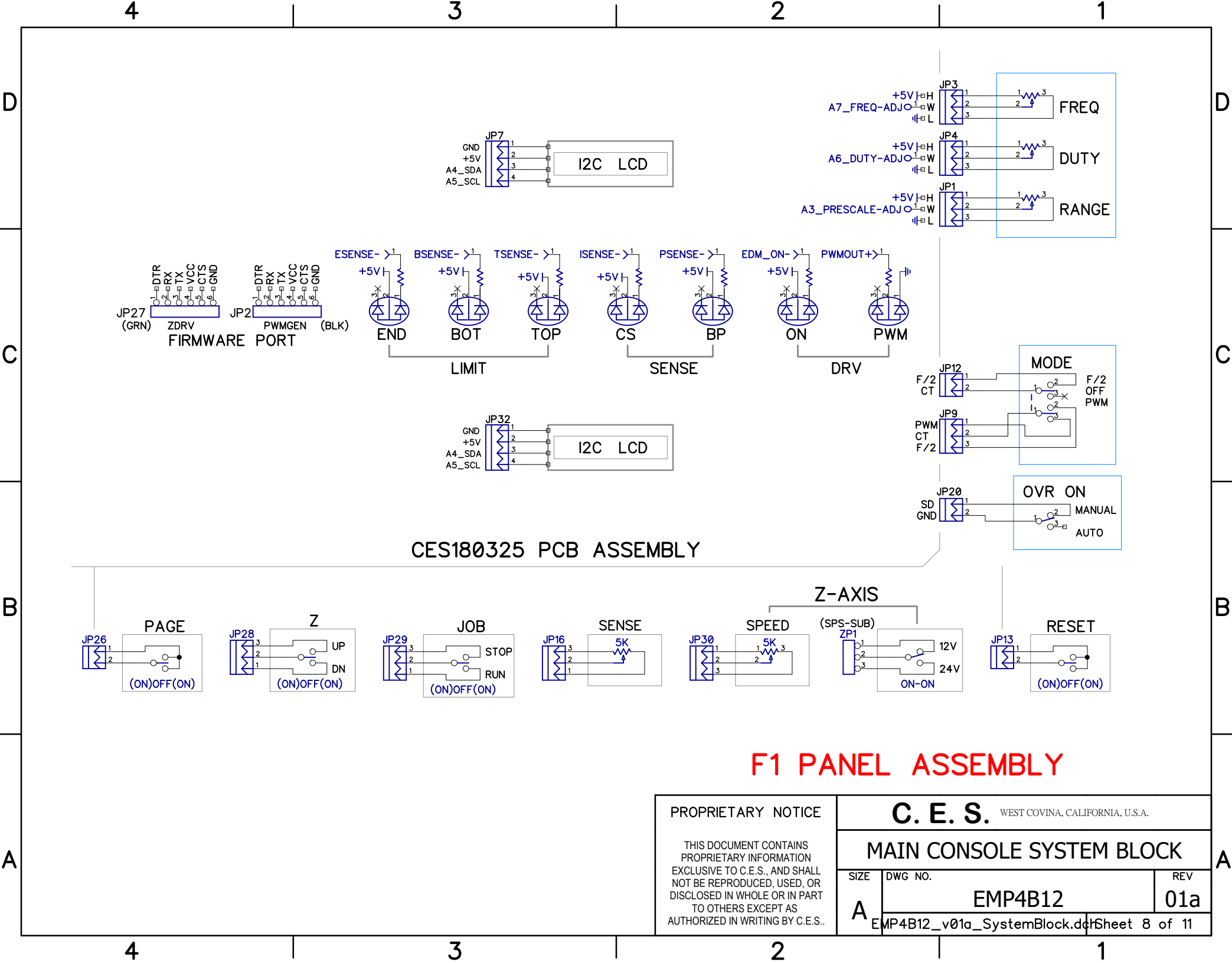
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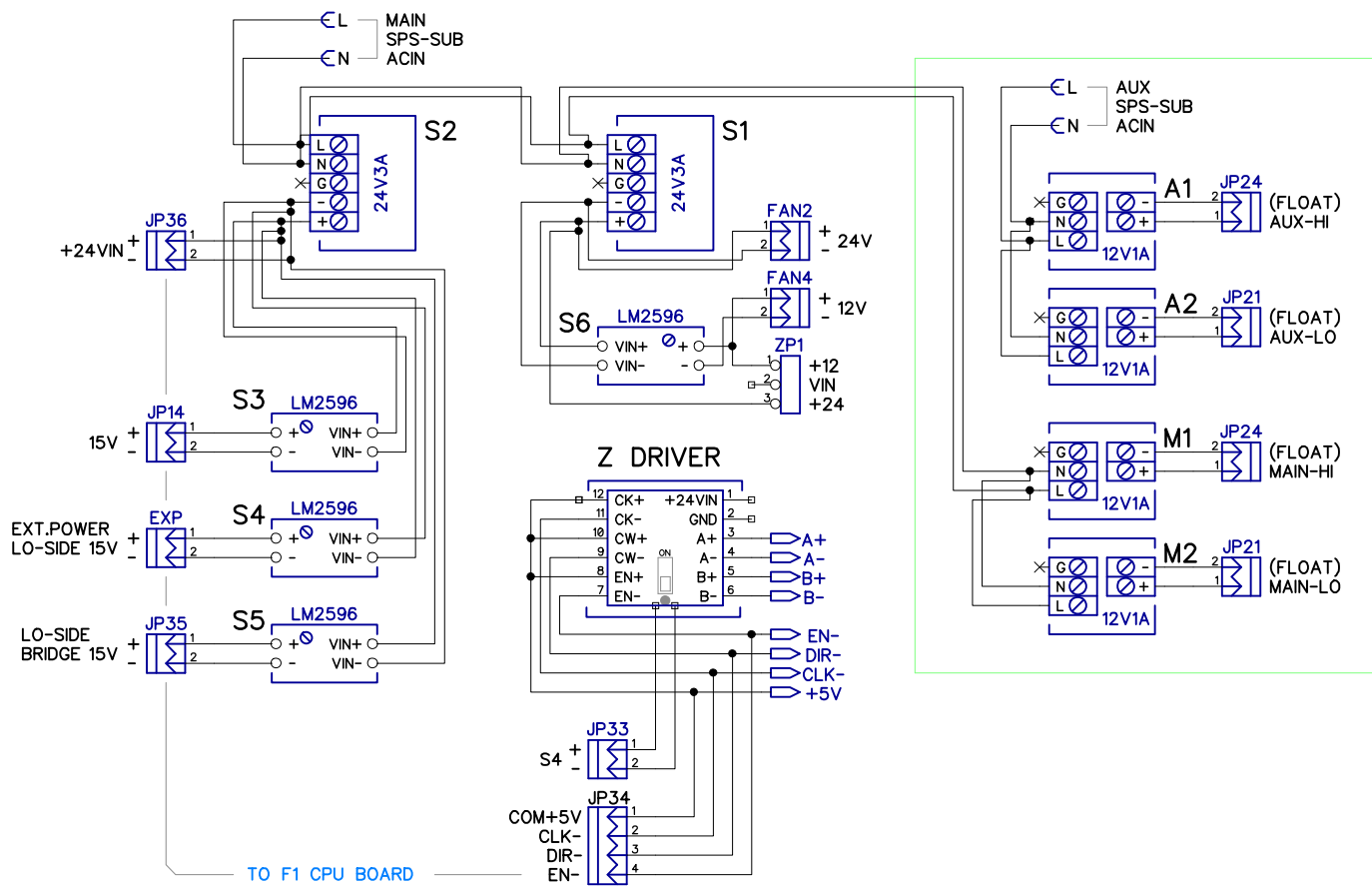
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MAIN CONSOLE SYSTEM BLOCK

SIZE	DWG NO.	REV
A	EMP4B12	01a
EMP4B12_v01a_SystemBlock.doc Sheet 7 of 11		



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	MAIN CONSOLE SYSTEM BLOCK		
	SIZE	DWG NO.	REV
	A	EMP4B12	01a
EMP4B12_v01a_SystemBlock.dwg Sheet 8 of 11			



SPS-SUB ASSEMBLY

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	MAIN CONSOLE SYSTEM BLOCK		
	SIZE A	DWG NO. EMP4B12	REV 01a
	EMP4B12_v01a_SystemBlock.doc Sheet 10 of 11		

4

3

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1

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D

C

C

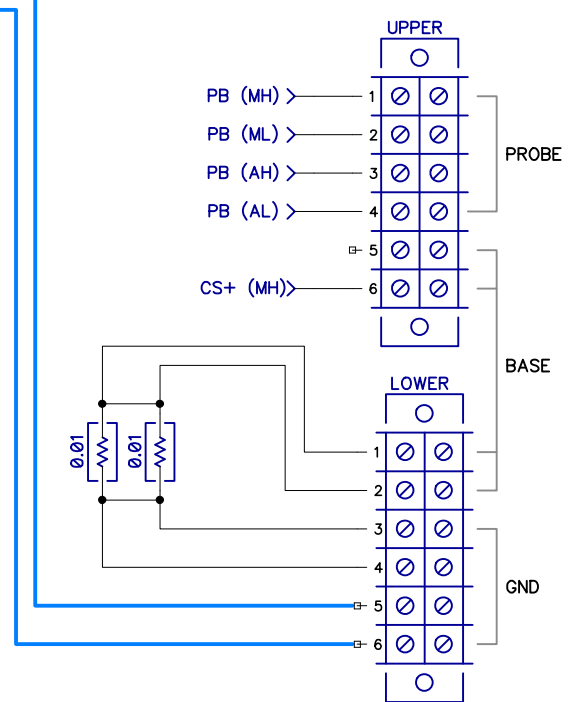
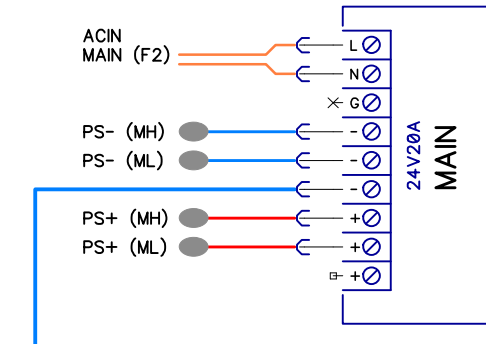
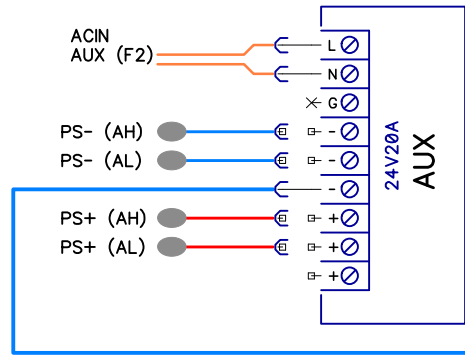
B

B

A

A

PB POWER SECTION



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MAIN CONSOLE SYSTEM BLOCK			
SIZE	DWG NO.		REV
A	EMP4B12		01a
EMP4B12_v01a_SystemBlock.dwg Sheet 11 of 11			